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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/716,529
Filing Date: November 20, 2003
Appellant(s): HOU, CHENG-LIANG (ANDREW)

Brad Y. Chin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/11/2008 appealing from the Office action mailed 12/11/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2003/0081624	Aggarwai et al.	05-2003
6137807	Rusu et al.	10-2000
7088730	Hsu et al.	08-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Rusu et al. (6137807).

Regarding claim 1, Rusu et al. disclose a dual bank queue memory and queue control system **(see column 1line 30-38)** comprising:

- receiving a packet **(see figure 5 box 305 cell input and column 2 line 28-29)**;
- determining an address of a free entry in a queue **(see figure 5 box 310 either bank 1 or 2 in use and 320 store and column 3 line 35-37 queue number)**;
- placing the determined address in an entry of a prior-determined address in the queue to form a linking list **(Rusu disclose control number which indicates start of packet, end of packet, normal cell in a packet, and abort (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue) and this control portion is established by the queue controller and contains link list pointers (or address) of the data (col. 4 lines 58-61) and it is inherent for an entry to be prior-determined address (col. 3 lines 37-38) where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link list is used to enable this operation, and keeps track of the mapping**

relationships (see col. 4 lines 58-67). Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list); and

- placing packet data of the packet in a free entry of a first data structure **(see figure 5 box 345 store cell in bank 1 and column 4 line 38-39)**,

wherein there is one-to-one mapping between the queue and the first data structure **(see column 3 line 51-53 and column 4 line 66)**.

Regarding claim 2, Rusu et al. teaches the packet is unicast **(see figure 1B box 116a MAC input – it is inherent that in MAC organizationally Unique Identifier (OUI) field has a indication of whether it is unicast or multicast)**.

Regarding claim 3, Rusu et al. teaches the packet is multicast **(see column 3 line 39 multicast)** or broadcast, and further comprising:

- determining an address of a free entry in each queue associated with a destination in the packet **(see column5 line 20-24 and figure 6 box 460 begin transmission of output from chosen bank)**; and
- for each queue associated with a destination in the packet, placing the respective determined address in a respective entry of a prior-determined address in each respective queue **(see figure 6 box 420 and column 5 line 28-29)**.

Regarding claim 4, Rusu et al. teaches further comprising:

- determining a priority level for the received packet **(see column 6 line 29 and figure 6 box 425 find highest priority queue having first cell in the chosen bank (per link list))**; and

- wherein the placing the determined address places the determined address in an entry of a prior-determined address in the queue having the same priority **(see column 5 line 25-30, and it is inherent that address places the determined address in an entry of a prior-determined address in the queue having the same priority)**.

Regarding claim 5, Rusu et al. teaches the determining a priority level includes examining a quality of service field within the received packet **(see column 5 line 25-30 different priorities serves different services)**.

Regarding claim 6, Rusu et al. teaches further comprising updating free entry data to indicate that the determined address is in use **(see figure 5 box 360 update free list for the respective output queue)**.

Regarding claim 7, Rusu et al. teaches further comprising:

- placing a packet length of the packet in a free entry of a second data structure **(see column 3 lines 12-13 housekeeping and encapsulation (such as ensuring packet size and producing parity) is then perform, and col. 3 lines 51-56 each queue memory is assigned a asset of linkage and mapping and at a processing components by the queue controller, where components include a queue writer pointer, a queue reader pointer, a cell counter, a differential counter, and a**

maximum queue length. therefore the queue component maximum queue length is assigned to the memory) ; and

- wherein there is one-to-one mapping between the first data structure **(see column 3 line 51-53 and column 4 line 66 and figure 5 box 345 store cell in bank 1)** and the second data structure **(see figure 5 box 340 store cell in bank 2)** .

Regarding claim 8, Rusu et al. disclose a transmit queue system **(see column 2 line 18-19)** comprising:

- means for receiving a packet **(see figure 5 box 305 cell input and column 2 line 28-29)**;
- means for determining an address of a free entry in a queue **(see figure 5 box 310 either bank 1 or 2 in use and 320 store and column 3 line 35-37 queue number)**;
- means for placing the determined address in an entry of a prior-determined address in the queue to form a linking list **(Rusu disclose control number which indicates start of packet, end of packet, normal cell in a packet, and abort (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue) and this control portion is established by the queue controller and contains link list pointers (or address) of the data (col. 4 lines 58-61) and it is inherent for an entry to be prior-determined address (col. 3 lines 37-38) where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link**

list is used to enable this operation, and keeps track of the mapping relationships (see col. 4 lines 58-67). Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list); and

- means for placing packet data of the packet in a free entry of a first data structure **(see figure 5 box 345 store cell in bank 1 and column 4 line 38-39),** wherein there is one-to-one mapping between the queue and the first data structure **(see column 3 line 51-53 and column 4 line 66).**

Note: the phrase "capable of" of "adapted to" recited in varies locations in claim 9 do not positively support claim limitations, therefore, the limitation after these phrases will not be considered as claimed limitations. However, the cited reference teaches the limitations (see rejection).

Regarding claims 9, Rusu et al. teaches transmit queue system, comprising:

- a first data structure capable of holding a plurality of packet data **(see figure 1A box 130 queue memory bank1)**;
- a queue capable of holding a linking list of addresses, the addresses having a one-to-one mapping **(see column 3 line 52 mapping)** with addresses in the first data structure **(see figure 2 box 102 link list management)**;
- a packet receiving engine capable of receiving a packet **(see figure 2 box 201 input arbiter)**;

- a free entry engine coupled to the packet receiving engine and capable of determining an address of a free entry in the queue **(see figure 4 box 146 free list RAM for Q1 and Q2)**;

- a transmit queue engine **(see figure 1 box 160output processor and figure 4 box 147 output port link list for q1 and q2)**, coupled to the queue **(see figure 1A box 130 and 131queue memory bank1&2)**, the packet receiving engine **(see figure 1A box 1 and 2 input subsystem)** and the free entry engine **(see col. 2 lines 33-41 queue controller 1A box 140)** , capable of placing the determined address in an entry of a prior-determined address in the queue to form a linking list **(Rusu disclose control number which indicates start of packet, end of packet, normal cell in a packet, and abort (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue) and this control portion is established by the queue controller and contains link list pointers (or address) of the data (col. 4 lines 58-61) and it is inherent for an entry to be prior-determined address (col. 3 lines 37-38) where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link list is used to enable this operation, and keeps track of the mapping relationships (see col. 4 lines 58-67). Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address**

in an entry of a prior-determined address in the queue to form a linking list); and

- a packet buffer engine **(see figure 2 box 104 queue buffer 1 controller)**, coupled to the first data structure, the packet receiving engine and the free entry engine, capable of placing packet data **(figure 2 ref 107)**of the packet in a free entry of the first data structure **(see figure 2 box 104 queue buffer 1 controller)**.

Regarding claims 10, Rusu et al. teaches a method, comprising:

- receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number)**;

- reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output demultiplexers to buffer and resegment the data from a chosen queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented)**, the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**;

- transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;
- reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and
- using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Regarding claim 11, Rusu et al. teaches further comprising:

- reading a packet length of the packet in a free entry of a second data structure **(see column 3 lines 12-13 housekeeping and encapsulation (such as ensuring packet size and producing parity) is then perform, and col. 3 lines 51-56 each queue memory is assigned a asset of linkage and mapping and at a processing components by the queue controller, where components include a queue writer pointer, a queue reader pointer, a cell counter, a differential counter, and a maximum queue length. therefore the queue component maximum queue length is assigned to the memory)**; and
- wherein there is one-to-one mapping between the first data structure **(see column 3 line 51-53 and column 4 line 66 and figure 5 box 345 store**

cell in bank 1) and the second data structure **(see figure 5 box 340 store cell in bank 2)**.

Regarding claim 12, Rusu et al. teaches the receiving receives an address **(see column 4 line 62-67)** for higher priority packet data before receiving an address for lower priority packet data **(see column 4 lines 25-28 the input processors to determine processing priorities, that is determined by the input processor with the highest priority, and column 5 lines 28-30 storing incoming data, utilizing the link list with the highest priority, therefore packet data are sorted with higher priority first and therefore the address of higher priority packet data is received before the lower ones)**.

Regarding claim 13, Rusu et al. teaches the packet data is multicast **(see column 3 line 39 multicast)** or broadcast and the transmitting transmits the packet data to a plurality of network nodes **(see column 3 lines 39-41 multicast mask is a 46 bit attachment to a packet for indicating that the packet can be transmitted or routed to anywhere)**.

Regarding claim 14, Rusu et al. teaches the packet is unicast **(see figure 1B box 116a MAC input – it is inherent that in MAC organizationally Unique Identifier (OUI) field has a indication of whether it is unicast or multicast)**.

Regarding claim 15, Rusu et al. teaches further comprising updating free entry data to indicate an address is free after the transmitting **(see figure 5 box 360 update free list for the respective output queue and figure 6 box 470 update link list and box 475 update free list)**.

Regarding claims 16, Rusu et al. teaches a transmit queue system **(see column 2 line 18-19)**, comprising:

- means for receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number)**;
- means for reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output demultiplexers to buffer and resegment the data from a chosen queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented)**, the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**;
- means for transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;
- means for reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and

- means for using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Note: the phrase "capable of" of "adapted to" recited in claim 17 line 5 do not positively support claim limitations, therefore, the limitation after these phrases will not be considered as claimed limitations. However, the cited reference teaches the limitations (see rejection).

Regarding claims 17, Rusu et al. teaches a transmit queue system **(see column 2 line 18-19)**, comprising:

- a first data structure capable of holding a plurality of packet data **(see figure 1A box 130 queue memory bank1)**;
- a queue capable of holding a linking list of addresses, the addresses having a one-to-one mapping **(see column 3 line 52 mapping)** with addresses in the first data structure **(see figure 2 box 102 link list management)**;
- a packet transmit engine **(see figure 2 box 202 output arbiter)**, coupled to the first data structure and the queue, capable of
    - receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number**;

- reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank)**;
- transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**;
- reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and
- using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

(10) Response to Argument

Appellant has itemized the arguments traversing the rejections of the appealed claims, each of which will be treated in turn.

35 USC § 102(b) - Claim 1

In pages 11-13, appellants argue that Rusu fails to disclose or suggest that **Rusu fails to disclose or suggest, at least, "placing the determined address in an entry of a prior-determined address in the queue to form a linking list," as recited in claim 1**

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu teaches, i**n the preferred**

embodiment, the Queue number (i.e. determined address) is a 14 bit tag indicating which queue memory (130, 131) the packet will be stored in (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue) and this control portion is established by the queue controller and contains link list pointers (or address) of the data **(Each queue memory (130, 131) is assigned a set of linkage (i.e. link list with associated prior-determined address) and mapping (i.e. an entry) and at a processing components by the queue controller (140) (i.e. an entry of a prior-determined address in the queue to form a linking list). Examples of these components include a queue write pointer (19 bits), a queue read pointer (19 bits) (column 3 lines 51-55);** and it is inherent for an entry to be prior-determined address **(col. 3 lines 37-38)** where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link list is used to enable this operation, and keeps track of the mapping relationships **(see col. 4 lines 58-67)**. Figure 5, Rusu further discloses that **data in the memory banks (130, 131) is maintained in the form of queues on a FIFO (first in, first out) basis, organized by a link list (102) maintained by the queue controller (140) with the control memory (145) (Rusu, col. 4, lines 47-57)**. Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and thus meets the limitation. This can be further seen in column 3-4, lines 57-4, where Rusu teaches, i**n the preferred embodiment, each multiplexer (120, 121) selectively receives incoming internal cells from associated input processors (101, 102) and sends those cells to the queue controller (140) which provides for storage of these cells**

to a specified location (i.e. determined address) in one of the queue memory banks (130, 131) via the input bus (600, 601). Thus, the present invention provides the simultaneous reading and writing (i.e. using linked list) from different queue banks (130, 131) in real time, including continuous bidirectional queue input and output, simultaneously (column 3-4, lines 57-4).

35 USC § 102(b) – Claim 2

Appellant argues (page 14, paragraph 3) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 2. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 2 is allowable.

35 USC § 102(b) – Claim 3

Appellant argues (page 15, paragraph 1) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 3. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 3 is allowable.

35 USC § 102(b) – Claim 4

Appellant argues (page 15, paragraph 3) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 4. However, Examiner respectfully disagrees with the

Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 4 is allowable.

35 USC § 102(b) – Claim 5

Appellant argues (page 16, paragraph 1) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 5. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 5 is allowable.

35 USC § 102(b) – Claim 6

Appellant argues (page 16, paragraph 3) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 6. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 6 is allowable.

35 USC § 102(b) – Claim 7

Appellant argues (page 16, last paragraph) that because Rusu fails to disclose the particular features recited in independent claim 1, Rusu also fails to disclose the features further defined in claim 7. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited

in claim 1. Thus Examiner disagrees with the Appellant's assertion that claim 7 is allowable.

35 USC § 102(b) – Claim 8

In pages 17-19, appellants argue that Rusu fails to disclose or suggest that "**means for placing the determined address in an entry of a prior-determined address in the queue to form a linking list".**

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu teaches, **In the preferred embodiment, the Queue number (i.e. determined address) is a 14 bit tag indicating which queue memory (130, 131) the packet will be stored in (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue)** and this control portion is established by the queue controller and contains link list pointers (or address) of the data **(Each queue memory (130, 131) is assigned a set of linkage (i.e. link list with associated prior-determined address) and mapping (i.e. an entry) and at a processing components by the queue controller (140) (i.e. an entry of a prior-determined address in the queue to form a linking list). Examples of these components include a queue write pointer (19 bits), a queue read pointer (19 bits) (column 3 lines 51-55);** and it is inherent for an entry to be prior-determined address **(col. 3 lines 37-38)** where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link list is used to enable this operation, and keeps track of the mapping relationships **(see col. 4 lines 58-67)**. Figure 5, Rusu further discloses that **data in the memory banks (130, 131) is maintained in the form of queues on a FIFO (first in, first out) basis, organized by**

a link list (102) maintained by the queue controller (140) with the control memory (145) (Rusu, col. 4, lines 47-57). Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and thus meets the limitation. This can be further seen in column 3-4, lines 57-4, where Rusu teaches, **in the preferred embodiment, each multiplexer (120, 121) selectively receives incoming internal cells from associated input processors (101, 102) and sends those cells to the queue controller (140) which provides for storage of these cells to a specified location (i.e. determined address) in one of the queue memory banks (130, 131) via the input bus (600, 601). Thus, the present invention provides the simultaneous reading and writing (i.e. using linked list) from different queue banks (130, 131) in real time, including continuous bidirectional queue input and output, simultaneously (column 3-4, lines 57-4).**

35 USC § 102(b) – Claim 9

In pages 21-23, appellants argue that Rusu fails to disclose or suggest that "**a transmit queue engine, couple to the queue, the packet receiving engine and the free entry engine, capable of placing the determined address in an entry of a prior-determined address in the queue to form a linking list.**"

In response, Rusu teaches, a transmit queue engine **(see figure 1 box 160 output processor and figure 4 box 147 output port link list for q1 and q2)**, coupled to the queue **(see figure 1A box 130 and 131 queue memory bank1&2)**, the packet receiving engine **(see figure 1A box 1 and 2 input subsystem)** and the free entry engine **(see col. 2 lines 33-41 queue controller 1A box 140)**, , **in the preferred**

embodiment, the Queue number (i.e. determined address) is a 14 bit tag indicating which queue memory (130, 131) the packet will be stored in (col.3 lines 37-38 corresponds to determining an address of a free entry in a queue) and this control portion is established by the queue controller and contains link list pointers (or address) of the data **(Each queue memory (130, 131) is assigned a set of linkage (i.e. link list with associated prior-determined address) and mapping (i.e. an entry) and at a processing components by the queue controller (140) (i.e. an entry of a prior-determined address in the queue to form a linking list). Examples of these components include a queue write pointer (19 bits), a queue read pointer (19 bits) (column 3 lines 51-55);** and it is inherent for an entry to be prior-determined address **(col. 3 lines 37-38)** where packet stream comes in and controller assigns either start of packet or end of packet according to the position of the stream, and the link list is used to enable this operation, and keeps track of the mapping relationships **(see col. 4 lines 58-67)**. Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and thus meets the limitation. Figure 5, Rusu further discloses that **data in the memory banks (130, 131) is maintained in the form of queues on a FIFO (first in, first out) basis, organized by a link list (102) maintained by the queue controller (140) with the control memory (145) (Rusu, col. 4, lines 47-57)**. Therefore this control number/address keeps track of the mapping relationships, which corresponds to placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and thus meets the limitation. This can be further seen in column 3-4, lines 57-4, where Rusu teaches, **in**

the preferred embodiment, each multiplexer (120, 121) selectively receives incoming internal cells from associated input processors (101, 102) and sends those cells to the queue controller (140) which provides for storage of these cells to a specified location (i.e. determined address) in one of the queue memory banks (130, 131) via the input bus (600, 601). Thus, the present invention provides the simultaneous reading and writing (i.e. using linked list) from different queue banks (130, 131) in real time, including continuous bidirectional queue input and output, simultaneously (column 3-4, lines 57-4).

35 USC § 102(b) - Claim 10

In pages 23-26, appellants argue that Rusu fails to disclose or suggest that **"receiving an address in a queue; reading packet data from an entry from a first data structure with the same address as the received address.., reading a next address in the queue from the received address in the queue; and using the next address to repeat the reading packet data and the transmitting," as recited in claim 10.**

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu teaches receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; here packet entry to the queue is addressed with control number)**; reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output**

demultiplexers to buffer and resegment the data from a chosen queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented), the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**; transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**; reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**. Examiner respectfully notes, in response to Appellant's argument that **Rusu fails to disclose or suggest "receiving an address in a queue",** Rusu in column 5 line 6-15 and column 4 lines 52-67 teaches control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number, and which meets the limitation **"receiving an address in a queue",** and rejection respectfully remains. Furthermore, Rusu discloses a cell in queue memory consisting of two parts, data and a control header. The control header is established by the queue controller and contains the link list pointers, or addresses, of the data, as illustrated in Figure 7. As shown in Figure 7, which illustrates a detailing control memory (145), the header portion (Q1, F1), may be stored in one queue memory location and the tail portion may be stored in another queue memory. The link list is used to enable this operation and keeps track of the mapping relationships (Rusu, col. 4, lines 58-67).

35 USC § 102(b) – Claim 11

Appellant argues (page 26, last paragraph) that because Rusu fails to disclose the particular features recited in independent claim 10, Rusu also fails to disclose the features further defined in claim 11. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 10. Thus Examiner disagrees with the Appellant's assertion that claim 11 is allowable.

35 USC § 102(b) – Claim 12

Appellant argues (page 27, paragraph 1) that because Rusu fails to disclose the particular features recited in independent claim 10, Rusu also fails to disclose the features further defined in claim 12. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 10. Thus Examiner disagrees with the Appellant's assertion that claim 12 is allowable.

35 USC § 102(b) – Claim 13

Appellant argues (page 27, last paragraph) that because Rusu fails to disclose the particular features recited in independent claim 10, Rusu also fails to disclose the features further defined in claim 13. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 10. Thus Examiner disagrees with the Appellant's assertion that claim 13 is allowable.

35 USC § 102(b) – Claim 14

Appellant argues (page 28, paragraph 1) that because Rusu fails to disclose the particular features recited in independent claim 10, Rusu also fails to disclose the features further defined in claim 14. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 10. Thus Examiner disagrees with the Appellant's assertion that claim 14 is allowable.

35 USC § 102(b) – Claim 15

Appellant argues (page 28, paragraph 4) that because Rusu fails to disclose the particular features recited in independent claim 10, Rusu also fails to disclose the features further defined in claim 15. However, Examiner respectfully disagrees with the Appellant's assertion. As shown above, Rusu does indeed teach all the features recited in claim 10. Thus Examiner disagrees with the Appellant's assertion that claim 15 is allowable.

35 USC § 102(b) - Claim 16

In pages 31, appellants argue that Rusu fails to disclose or suggest that **at least, "means for receiving an address in a queue; means for reading packet data from an entry from a first data structure with the same address as the received address.., means for reading a next address in the queue from the received address in the queue; and means for using the next address to repeat the reading packet data and the transmitting," as recited in claim 16.**

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu teaches a transmit queue

system **(see column 2 line 18-19)**, comprising: means for receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number)**; means for reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output from chosen bank and column 5 lines 31-34 the output arbitration subsystem coordinates the output demultiplexers to buffer and resegment the data from a chosen queue memory into an acceptable concatenated form for output, and it is inherent that the packet data to be read for it to be resegmented)**, the queue and the first data structure having one-to-one mapping **(see column 3 line 51-52)**; means for transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**; means for reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and means for using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Appellant argues (page 31 paragraph 2) Rusu fails to disclose or suggest at least "**means for receiving an address in a queue**."

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu in column 5 line 6-15 and column 4 lines 52-67 teaches control memory is addressed under the control of the

input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number, and which meets the limitation "receiving an address in a queue", and rejection respectfully remains.

35 USC § 102(b) - Claim 17

In pages 35, appellants argue that Rusu fails to disclose or suggest that **at least, "a packet transmit engine...capable of receiving an address in a queue; reading packet data from an entry from a first data structure with the same address as the received address.., reading a next address in the queue from the received address in the queue; and using the next address to repeat the reading packet data and the transmitting," as recited in claim 17.**

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu teaches a transmit queue system **(see column 2 line 18-19)**, comprising: a first data structure capable of holding a plurality of packet data **(see figure 1A box 130 queue memory bank1)**; a queue capable of holding a linking list of addresses, the addresses having a one-to-one mapping **(see column 3 line 52 mapping)** with addresses in the first data structure **(see figure 2 box 102 link list management)**; a packet transmit engine **(see figure 2 box 202 output arbiter)**, coupled to the first data structure and the queue, capable of receiving an address in a queue **(see column 5 line 6-15 and column 4 lines 52-67 control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number**; reading packet data from an entry from a first data structure with the same address as the received address **(see figure 6 box 460 begin transmission of output**

from chosen bank); transmitting the packet data to a network node associated with the queue **(see column 2 line 32 output processor to provide respective output, and it is inherent that packet data will be transmitted to a node which has a memory or queue)**; reading a next address in the queue from the received address in the queue **(see figure 7 link lists b1 pointer location to q1)**; and using the next address to repeat the reading packet data and the transmitting **(see column 4 line 65-67 and figure 6 box 460 begin transmission of output from chosen bank)**.

Appellant argues (page 31 paragraph 2) Rusu fails to disclose or suggest "**a packet transmit engine…capable of receiving an address in a queue**."

However, Examiner respectfully disagrees with the Appellant's assertion. Rusu does indeed teach the cited limitations. Specifically, Rusu in column 5 line 6-15 and column 4 lines 52-67 teaches control memory is addressed under the control of the input arbitrator and the output arbitrator; where packet entry to the queue is addressed with control number, and which meets the limitation "receiving an address in a queue", and rejection respectfully remains. Examiner respectfully **Notes: the phrase "capable of" of "adapted to" recited in claim 17 line 5 do not positively support claim limitations, therefore, the limitation after these phrases will not be considered as claimed limitations. However, the cited reference teaches the limitations (see rejection).**

For the above reasons, it is believed that the rejections should be sustained.

(11) Evidence Appendix

No evidence was provided by appellant.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/S. A./
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